REMARKS/ARGUMENTS

The foregoing amendment and the following arguments are provided to impart precision to the claims, by more particularly pointing out the invention, rather than to avoid prior art.

Drawings

A proposed drawing correction of Figures 19 and 20 is enclosed. The correction does not incorporate any new matter, since both Figures 19 and 20 are described in detail in the specification.

Further, the "read request within a write packet" of claims 2, 11, and 14 is shown in Figure 8. Figure 8 illustrates a write packet 818. Within the write packet 818 are several flits, including a read request flit 810. Therefore, this feature of the claims is shown in the drawings.

Claim Objections

Claim 7 was objected to because of the following informalities: On line 8, "a processor having an memory output" should be -- a processor having a memory output—. Claim 7 has been amended to overcome the Examiner's objection.

35 U.S.C. § 112 Rejections

Claims 2, 11, and 14 were rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Paragraph 58 of the specification describes a write packet having a read request packet flit incorporated therein. This feature is also shown as element

810 of Figure 8. A write packet could incorporate any of several different types of flits, including a read request flit. As a result, claims 2, 11, and 14 are not indefinite, and are enabled.

35 U.S.C. § 102(e) Rejections

Examiner rejected claims 1, 3-10, 12-13, and 15-37 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,266,747 (hereinafter "Dahl").

As amended, claim 1 reads as follows:

> A method comprising:
>
> receiving a write request in parts;
>
> receiving a read request; and
>
> preempting transfer of write data with the read request by not completing the write request until all of the parts of the write request are received.

Dahl does not teach all the limitations of claim 1, and as a result does not anticipate claim 1. Specifically, Dahl does not teach preempting transfer of write data with the read request by not completing the write request until all of the parts of the write request are received. Instead, Dahl teaches a read priority system, where read requests have priority over write requests (Col. 2, lines 52-55). Dahl implements this system by using separate read and write queues (Col. 3, lines 8-10), and fulfilling the requests from the read queue before fulfilling the requests from the write queue (Col. 2, lines 53-59). Therefore, Dahl assigns priority to read requests and issues the read requests before the write requests unless a read request depends on a write request (Col. 2, lines 55-59). As a result,

Dahl does not teach preempting transfer of write data with the read request by not completing the write request until all of the parts of the write request are received, as in claim 1, and claim 1 is patentable over Dahl, since each of the write requests in the write request queue is complete, and since Dahl continues to process read requests even if complete write requests are available.

Independent claims 10, 13, and 16 include limitations similar to the limitation of claim 1 discussed above. Therefore, for the same reasons as discussed above regarding claim 1, claims 10, 13, and 16 are also not anticipated by Dahl.

Claims 2-6, 11-12, 14-15, and 17-18 depend from the above discussed independent claims, and as a result include all the limitations of those independent claims. Since the independent claims are not anticipated by Dahl, claims 2-6, 11-12, 14-15, and 17-18 are also not anticipated by Dahl.

Claim 7, as amended, includes a limitation of wherein a memory port has a memory port protocol allowing a processor write request received in parts to be preempted by a processor read request by not completing the write request until all of the parts of the write request are received. As mentioned above, Dahl does not teach preempting write data with the read request by not completing the write request until all of the parts of the write request are received. Therefore, claim 7 is not anticipated by Dahl.

Claim 9 depends from claim 7 and therefore includes all the limitations of claim 7. Since claim 7 is not anticipated by Dahl, claim 9 is also not anticipated by Dahl.

As amended, claim 19 reads as follows:

A method comprising:

receiving a read request flit; and

dispatching an early read request from the request flit to a memory during the receiving.

As mentioned above, Dahl teaches two separate queues of read and write requests. Dahl does not teach that a read request may be dispatched during the receiving of a flit, as in claim 19. Instead, Dahl teaches that read requests are generally given priority over write requests. Dahl also teaches that under a pre-fetching technique, newly arrived instructions are fetched prior to the execution of a previous instruction (Col. 3, lines 3-10). However, this only means that the instructions are fetched, and not that a read request is dispatched, as in claim 19. Dahl does not mention dispatching a request from a request flit *while* receiving the request flit as in the claims. As a result, claim 19 is not anticipated by Dahl.

Claims 23, 26, 29, 32, and 35 include limitations similar to those in claim 19. As a result, claims 23, 26, 29, 32, and 35 are also not anticipated by Dahl. Claims 25, 27-28, 30-31, 33-34, and 35-36 depend from the above discussed independent claims. Since the independent claims are not anticipated by Dahl, claims 25, 27-28, 30-31, 33-34, and 35-36 are also not anticipated by Dahl.

CONCLUSION

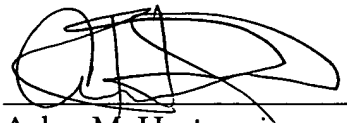
Applicants respectfully submit the present application is in condition for allowance. If the Examiner believes a telephone conference would expedite or assist in the allowance of the present application, the Examiner is invited to call Arlen M. Hartounian at (408) 720-8300.

Authorization is hereby given to charge our Deposit Account No. 02-2666 for any charges that may be due.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN

Date: 6/28/04



Arlen M. Hartounian
Reg. No. 52,997

12400 Wilshire Boulevard
Seventh Floor
Los Angeles, CA 90025-1026
(408) 720-8300

1800

LL signals	Transfers 0:3
0	Tag, Control, and Check Bits
1	
2	Tag, Info, and Check Bits
3	

FIG. 18

1900

LLSignals	Transfers 0:3
0	Tag and Check Bits
1	
2	Tag, Info, and Check Bits
3	

FIG. 19

2000

LL signals	Transfers 0:3
0	Signal and Check Bits
1	
2	Signal, Info, Stop, and Check Bits
3	

FIG. 20